REMARKS

Claims 1-6 and 8-25 are pending in the present application. The specification has been amended to provide textual support for the claim amendments entered in Applicant's prior response, dated August 29, 2001. Support for each of the amendments to the specification can be found in Figures 9 and 14-16. Accordingly, favorable reconsideration of the pending claims is respectfully requested.

Applicants have submitted herewith an amended substitute drawing sheet for Figure 16 and a copy of the drawing sheet showing proposed changes for Figure 16 to correct a typographical error in the reference numerals. In particular, one instance of the number "52" has been changed to "50" as indicated in Figure 16. Support for these changes to Figure 16 can be found on page 16, line 8 of the application as filed. Accordingly, entry of the amended substitute drawing sheet is respectfully requested.

1. Rejections Under 35 U.S.C. § 112

Claims 1-6 and 8-22 are rejected under 35 U.S.C. § 112, first paragraph, as containing subject matter not described in the specification in such a way as to enable one skilled in the art to make and/or use the invention. In particular, the Examiner has indicated that the limitation of the sleeve insulator comprising a first and second terminus is not adequately described in the specification. Applicants respectfully traverse.

In response, Applicants have amended the specification at the paragraphs beginning at page 11, line 7; page 14, line 17; page 15, line 15; and at page 16, line 3 to provide support for the recited limitations regarding the sleeve insulator comprising a first terminus and a second terminus. Support for the amendments can be found throughout the drawings, in particular through an inspection of

sleeve insulator layers 50, 52, and 53 in Figures 9 and 14-16. Accordingly, the prompt removal of this rejection under 35 U.S.C. § 112, first paragraph is respectfully requested.

2. Rejections Under 35 U.S.C. § 102

Claims 1-6, 8-10, and 12-21 have been rejected under 35 U.S.C. § 102(e) as being anticipated by U.S. Patent No. 6,165,839 to Lee et al (hereinafter "*Lee*"). Applicants respectfully traverse.

Lee discloses silicon nitride spacers 26 on the sides of a bit line contact hole, extending from and adjacent a top silicon nitride layer 22 at a first terminus, adjacent an interlayer dielectric layer 21, and adjacent a cell plate structure (Figure 15). The spacers 26 have a second terminus adjacent a silicon nitride layer 10 and at the top of a lower bulk insulator layer 9.

Independent claims 1, 13, and 15 recite that the sleeve insulator layer has a first terminus adjacent to the conductor layer, and a second terminus opposite the first terminus and within the lower bulk insulator layer. In contrast, *Lee* discloses that spacers 26 have a first terminus adjacent top silicon nitride layer 22 (not a conductor layer), and a second terminus at the top of bulk insulator layer 9.

Independent claim 19 recites that the sleeve insulator layer has a first terminus adjacent the capacitor cell plate, and a second terminus opposite the first terminus and in contact with the capacitor storage node. In contrast, *Lee* discloses that spacers 26 have a first terminus adjacent top silicon nitride layer 22 (not a capacitor cell plate), and a second terminus at the top of bulk insulator layer 9 which contacts silicon nitride layer 10 and polysilicon layer 20a (not capacitor storage nodes).

Accordingly, for at least the above reasons, Applicants submit that claims 1, 13, 15, and 19, as well as dependent claims 2-6, 8-10, 12, 14, 16-18, and 20-21 are not anticipated by *Lee*. Applicants therefore respectfully request that the rejection of claims 1-10 and 12-21 under 35 U.S.C.

§102(e) be withdrawn.

Claims 1-6, 8-10, and 13-18 have been rejected under 35 U.S.C. § 102(e) as being anticipated by U.S. Patent No. 5,973,910 to Gardner (hereinafter "*Gardner*") for the reasons set forth on page 3 of the Office Action. Applicants respectfully traverse.

Gardner discloses a structure in which a sidewall insulator 107 has a first terminus adjacent to the top of an insulative layer 105, and extends to the top of substrate 100 at a second terminus (Figure 2). A pair of capacitor conductor layers 102 and 104 both contact insulator 107, and a conductive contact 108 terminates at the top of substrate 100.

Independent claims 1, 13 and 15 recite that the sleeve insulator layer has a first terminus adjacent to the conductor layer, and a second terminus opposite the first terminus and above the semiconductor substrate. In contrast, *Gardner* discloses that insulator 107 has a first terminus adjacent to the top of insulative layer 105 (not a conductor layer), and a second terminus at substrate 100. Further, Applicants note that claims 1, 13, and 15 also recite that the conductive contact or plug extends beyond the sleeve insulator layer to terminate at a contact on the substrate. In contrast, *Gardner* discloses that insulator 107 and conductive contact 108 both terminate at the top of substrate 100.

Accordingly, Applicants submit that claims 1-6, 8-10, and 13-18 are not anticipated by *Gardner*. Applicants therefore respectfully request that the rejection of these claims under 35 U.S.C. §102(e) be withdrawn.

Claims 19-21 have been rejected under 35 U.S.C. § 102(b) as being anticipated by U.S. Patent No. 5,475,247 to Kim (hereinafter "*Kim*") for the reasons set forth on page 3 of the Office Action. Applicants respectfully traverse.

Kim is directed to a manufacturing process for providing a contact structure, and discloses an insulating layer 15' on the sidewall of a contact opening. *Kim* depicts the insulating layer as having a first terminus adjacent the top edge of a third dielectric layer 13, which is disposed over a second dielectric layer, which overlies a capacitor cell plate conductor layer 8 and an insulator 7 (Figure 3).

Independent claim 19 recites that the sleeve insulator layer has a first terminus adjacent the capacitor cell plate, and a second terminus opposite the first terminus and in contact with the capacitor storage node. In contrast, *Kim* discloses that insulating layer 15' has a first terminus adjacent the top edge of dielectric layer 13 (not a capacitor cell plate). In addition, the second terminus of insulating layer 15' does not appear to be in contact with a capacitor storage node as recited in claim 19.

Accordingly, Applicants respectfully assert that claims 19-21 are not anticipated by *Kim*. Applicants therefore respectfully request that the rejection of these claims under 35 U.S.C. § 102(b) be withdrawn.

3. Rejections Under 35 U.S.C. § 103(a)

Claims 11 and 12 have been rejected under 35 U.S.C. § 103(a) as being unpatentable over *Gardner* in view of U.S. Patent No. 5,338,700 to Dennison et al. (hereinafter "*Dennison*") and U.S. Patent No. 6,198,143 B1 to Ohsaki (hereinafter "*Ohsaki*") for the reasons set forth on pages 4-5 of the Office Action. Applicants respectfully traverse.

Claims 11 and 12 depend from claim 1 and thus include contain the limitations thereof. As discussed, claim 1 recites that the sleeve insulator layer has a first terminus adjacent to the conductor layer, and a second terminus opposite the first terminus and above the semiconductor substrate. Further, claim 1 recites that the conductive contact extends beyond the sleeve insulator layer to

terminate at a contact on the substrate.

There is no teaching or suggestion in *Gardner* of these recitations in present claim 1. Rather, *Gardner* discloses that insulator 107 has a first terminus adjacent to the top of insulative layer 105 (not a conductor layer), and a second terminus at substrate 100. *Gardner* also discloses that insulator 107 and conductive contact 108 both terminate at the top of substrate 100. There is also no teaching or suggestion in *Dennison* or *Ohsaki* of these recitations in claim 1. For example, *Dennison* does not even disclose a sleeve insulator layer for a contact structure, while *Ohsaki* discloses an insulator 92 having a first terminus adjacent to the top of an insulating layer 78 (not a conductor layer).

Thus, even if the teachings of these cited references are combined, not all of the limitations of claims 11 and 12 would be met. Accordingly, Applicants submit that claims 11 and 12 would not have been obvious over the cited references. Applicants therefore respectfully request that the rejection of these claims under 35 U.S.C. § 103(a) be withdrawn.

Claims 22-25 have been rejected under 35 U.S.C. § 103(a) as being unpatentable over *Lee* in view of *Ohsaki* for the reasons set forth on pages 5-6 of the Office Action. Applicants respectfully traverse.

Independent claim 22 recites that the sleeve insulator layer has a first terminus adjacent to and in contact with the conductor layer, and a second terminus above the semiconductor substrate and within the lower bulk insulator layer. There is no teaching or suggestion in *Lee* of these recitations in present claim 1. Rather, *Lee* discloses that spacers 26 have a first terminus adjacent top silicon nitride layer 22 (not a conductor layer), and a second terminus at the top of bulk insulator layer 9. There is also no teaching or suggestion in *Ohsaki* of these recitations in claim 22. Rather, *Ohsaki* discloses an insulator 92 having a first terminus adjacent to the top of an insulating layer 78 (not a conductor layer).

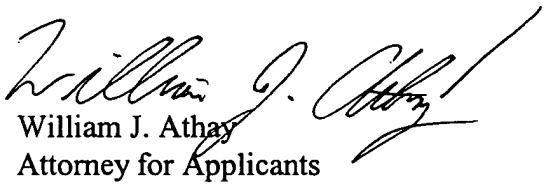
Thus, even if the teachings of *Lee* and *Ohsaki* are combined, not all of the limitations of claim 22 and dependent claims 23-25 would be met. Therefore, Applicants submit that claims 22-25 would not have been obvious over the cited references. Applicants therefore respectfully request that the rejection of these claims under 35 U.S.C. § 103(a) be withdrawn.

CONCLUSION

In view of the foregoing, Applicants respectfully request favorable reconsideration and allowance of the present claims. In the event the Examiner finds any remaining impediment to the prompt allowance of this application which could be clarified by a telephone interview, the Examiner is respectfully requested to contact the undersigned attorney.

Dated this 2nd day of April 2002.

Respectfully submitted,



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VERSION WITH MARKINGS TO SHOW THE CHANGES MADE

In the Specification:

The paragraph beginning at page 11, line 7 has been amended as follows:

Referring to Figure 9, a second etch step, which is anisotropic, is carried out to remove substantially all of the horizontally-exposed portions of sleeve insulator layer 50 from the bottom of the partially formed BLCC. Sleeve insulator layer 50 thus covers the exposed portions of capacitor cell dielectric layer 44, cell plate layer 46, and cell plate insulating layer 48 that are within contact hole 70. As illustrated in Figure 9, sleeve insulator layer 50 thus has a first terminus substantially adjacent to cell plate layer 46 and cell plate insulating layer 48. Sleeve insulator layer 50 also has a second terminus opposite the first terminus, the second terminus being located below capacitor cell dielectric layer 44 and within lower bulk insulator layer 36.

The paragraph beginning at page 14, line 17 has been amended as follows:

Referring to Figure 14, a circle 80 illustrates in phantom a cross-section of an etch hole through upper bulk insulator layer 51. A center line 80 represents an axis passing through the center of circle 80. In Figure 14, center line 71 represents the axis passing through the center of sleeve insulator layer 50. The symbol Δ_3 represent the misalignment from the center of circle 80 to the center of sleeve insulator layer 50. As with sleeve insulator layer 50 in Figure 9, sleeve insulator layer 50 in Figure 14 has a first terminus substantially adjacent to cell plate layer 46 and cell plate insulating layer 48. Sleeve insulator layer 50 also has a second terminus opposite the first terminus, the second terminus being located below capacitor cell dielectric layer 44 and within lower bulk insulator layer 36.

The paragraph beginning at page 15, line 15 has been amended as follows:

The process creating the structure seen in Figure 14 is substantially the same as that creating the structure seen in Figure 15. In Figure 15, a circle 90 illustrates in phantom a cross-section of an etch hole through upper bulk insulator layer 51. The etch hole is aligned with respect to sleeve insulator layer 50. As with sleeve insulator layer 50 in Figure 9, sleeve insulator layer 50 in Figure 15 has a first terminus substantially adjacent to cell plate layer 46 and cell plate insulating layer 48. Sleeve insulator layer 50 also has a second terminus opposite the first terminus, the second terminus being located below capacitor cell dielectric layer 44 and within lower bulk insulator layer 36. Also, the etch is self aligned with sleeve insulator layer 50 due to the selectivity of the etch with respect to the material from which sleeve insulator layer 50 is substantially composed, and due to the etch selectivity to the material of which cell plate insulating layer 48 is composed. As was described with respect to Figure 13, the self-alignment of the etch through sleeve insulator layer 50 in effect assures electrical insulation of cell plate layer 46 to prevent an electrical short with electrically conductive bit line contact 92 within the BLCC. Figure 15 illustrates the maximum contact size on active area 18b, as dictated by the diameter of the area defined within sleeve insulator layer 50. Electrical insulation protection of bit line contact 92 is provided by cell plate insulating layer 48 and sleeve insulator layer 50 so as to prevent shorting of cell plate layer 46 with bit line contact 92.

The paragraph beginning at page 16, line 3 has been amended into three paragraphs as follows:

Figure 16 shows the divergent types of contacts that can be made using the invention, although all of the depicted contacts need not be present in the same structure nor be situated as depicted in Figure 16. In Figure 16, circle 90 illustrates in phantom a cross-section of an etch hole, made by conventional etch processes, through upper bulk insulator layer 51. A contact plug 72 in upon source/drain region 18b. Electrically conductive bit line contact 92 is situated within contact hole 70 and passes through sleeve insulator layer to terminate upon contact plug 72. As with sleeve insulator layer 50 in Figure 9, sleeve insulator layer 50 in Figure 16 has a first terminus substantially adjacent to cell plate layer 46 and cell plate insulating layer 48. Sleeve insulator layer 50 also has a second terminus opposite the first terminus, the second terminus being located below capacitor cell dielectric layer 44 and within lower bulk insulator layer 36.

Circle 94 illustrates in phantom a cross-section of a contact hole 98, made by conventional etch processes, through upper bulk insulator layer 51 and into a transistor stop on a gate 24 beneath an insulating protective layer 28 of a transistor. Electrically conductive contact 100 is situated within ~~contact hole 98 and passes through a sleeve insulator layer 52 to make contact with gate 24.~~ Sleeve insulator layer 52 in Figure 16 has a first terminus substantially adjacent to cell plate layer 46 and cell plate insulating layer 48. Sleeve insulator layer 52 also has a second terminus opposite the first terminus, the second terminus being located below capacitor cell dielectric layer 44, within lower bulk insulator layer 36, and in contact with storage node layer 42.

Circle 104 illustrates in phantom a cross-section of a contact hole 106, made by conventional etch processes, through upper bulk insulator layer 51 and into storage node layer 42. Electrically conductive contact 102 is situated within contact hole 106 and passes through a sleeve insulator layer 53 to make contact with storage node layer 42. Sleeve insulator layer 53 insulates electrically conductive contact 102 from cell plate layer 46. Sleeve insulator layer 53 in Figure 16 has a first terminus substantially adjacent to cell plate layer 46 and cell plate insulating layer 48. Sleeve insulator layer 53 also has a second terminus opposite the first terminus, the second terminus being located below capacitor cell dielectric layer 44 and in contact with storage node layer 42.